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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/783,007	02/15/2001	Junji Fujino	P103213-00020	1276	
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ARENT FOX KINTNER PLOTKIN & KAHN, PLLC Suite 600 1050 Connecticut Avenue, N.W.			EXAM	EXAMINER	
			YAM, STEPHEN K		
Washington, DC 20036-5339			ART UNIT	PAPER NUMBER	
			2878		
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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

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	Application No.	Applicant(s)	/			
	09/783,007	FUJINO, JUNJI	V			
Office Action Summary	Examiner	Art Unit	<u> </u>			
•	Stephen Yam	2878				
The MAILING DATE of this communication app	1 '		idress			
Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPL' THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.1: after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period v - Failure to reply within the set or extended period for reply will, by statute - Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b). Status	36(a). In no event, however, y within the statutory minimu will apply and will expire SIX , cause the application to be	, may a reply be timely filed m of thirty (30) days will be considered time (6) MONTHS from the mailing date of this o come ABANDONED (35 U.S.C. § 133).	ly. communication.			
1) Responsive to communication(s) filed on 25 h	-ebruary 2003 .					
2a) ☐ This action is FINAL . 2b) ☑ Th	is action is non-final	l.				
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims	Ex parte Quayle, 19	33 C.D. 11, 433 O.G. 213.				
4)⊠ Claim(s) <u>1,2,4-9 and 11-15</u> is/are pending in t	he application.					
4a) Of the above claim(s) is/are withdrawn from consideration.						
5)☐ Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1,2,4-9 and 11-15</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/o Application Papers	r election requireme	ent.				
9)☐ The specification is objected to by the Examine	r.					
10)☐ The drawing(s) filed on is/are: a)☐ acce	pted or b)☐ objected	to by the Examiner.				
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
11)☐ The proposed drawing correction filed on is: a)☐ approved b)☐ disapproved by the Examiner.						
If approved, corrected drawings are required in reply to this Office action.						
12)☐ The oath or declaration is objected to by the Ex	aminer.					
Priority under 35 U.S.C. §§ 119 and 120						
13) Acknowledgment is made of a claim for foreig	n priority under 35 U	J.S.C. § 119(a)-(d) or (f).				
a) ☐ All b) ☐ Some * c) ☐ None of:						
1. Certified copies of the priority document	s have been receive	ed.				
2. Certified copies of the priority document	s have been receive	ed in Application No				
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).						
a) ☐ The translation of the foreign language provisional application has been received. 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.						
Attachment(s)						
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) 🔲 N	nterview Summary (PTO-413) Paper N lotice of Informal Patent Application (P ther:				
U.S. Patent and Trademark Office PTO-326 (Rev. 04-01) Office A	ction Summary	Part o	of Paper No. 12			

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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

- 1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 8, 2003 has been entered.
- 2. Claims 1, 2, 4-9, and 11-15 are currently pending.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

4. Claims 1 and 14 are objected to because of the following informalities:

In Claim 1, a period is required at the end of the claim.

In Claim 1, line 7, "their electric signal" is unclear, as it is unclear whether the term is identical to "the electric signal".

In Claim 14, line 1, "claimed" is misspelled as "chimed".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

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5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 6. Claims 1, 4-7, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuda et al. US Patent No. 4,629,882.

Regarding Claims 1 and 9, Matsuda et al. teach (see Fig. 4) a photoelectric conversion and amplification device comprising a photoelectric conversion element (20), a first electrode (30a) connected electrically to the photoelectric conversion element and by which the electric signal is extracted from the photoelectric conversion element, a second electrode (30c) formed on the photoelectric conversion element in close proximity to the first electrode in such a way that the electric signal (out of 30a) does not pass through the second electrode, an amplifier circuit (52) (see Col. 6, lines 23-29) with a first input terminal (32a) and a second input terminal (32c) and amplifying and outputting a difference between electric signals fed to the first and second input terminals (see Col. 6, lines 23-29), a first bonding wire (26a) (see Fig. 3a and 3b) connecting the first electrode to the first input terminal and a second bonding wire (26c) having a substantially identical length as and laid substantially parallel to the first bonding wire, connecting the second electrode to the second input terminal. Regarding claim 9, "an infrared communication device" cannot be given any patentable weight since the body of the claim does not claim such structure.

Regarding Claim 4, Matsuda et al. teach a distance between the first electrode and the first input terminal and a distance between the second electrode and the second input terminal as

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substantially identical (see Fig. 3a and 3b) and a distance between the first and second electrodes and a distance between the first and second input terminals as "substantially" similar.

Regarding Claim 5, Matsuda et al. teach the photoelectric conversion element including a photodiode (see Col. 4, lines 28-33) built by joining an N-type semiconductor (22) and a P-type semiconductor (24) together, and the first electrode is connected electrically to one end of the photodiode.

Regarding Claim 6, Matsuda et al. teach the photoelectric conversion element including a photodiode (see Col. 4, lines 28-33) comprised of joining an N-type semiconductor (22) and a P-type semiconductor (24) together and a diode comprised of joining an N-type semiconductor (22) and a P-type semiconductor (26) together and shielded from light (see Col. 5, lines 31-37), and the first electrode is connected electrically to one end of the photodiode and the second electrode is connected to one end of the diode (see Fig. 3b).

Regarding Claim 7, Matsuda et al. also teach (see Fig. 3b) a substrate (36) on which the photoelectric conversion circuit and the amplifier circuit are mounted, a first conductor pattern (strip of (32a)) and a second conductor pattern (strip of (32c)) formed on the substrate, where the first bonding wire connects the first electrode to the first input terminal (left end of (32a)) by way of the first conductor pattern (strip of (32a)) and the second bonding wire connects the second electrode to the second input terminal (right end of (32c)) by way of the second conductor pattern (strip of (32c)).

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Claim Rejections - 35 USC § 103

- 7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda et al. in view of Sawada et al. US Patent No. 5,652,425.

Matsuda et al. teach the device as taught in Claim 1, according to the appropriate paragraph above. Matsuda et al. do not teach identical bias voltages applied to the first and second input terminals. Sawada et al. teach (see Fig. 1) a photosensor-amplifier device comprising a photoelectric conversion element (1,5) and amplifier circuit (600) (see Fig. 3) with a first input terminal (V_{in1}) and a second input terminal (V_{in2}) wherein identical bias voltages (V_{PD}) are applied to the first and second input terminals (see Fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply identical bias voltages to the first and second input terminals as taught by Sawada et al. in the device of Matsuda et al., to provide identical noise signals into both input terminals of the amplifier to remove the noise component of the photodetection signal as taught by Sawada et al. (see Col. 3, lines 3-6 and Col. 4, lines 39-44).

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda et al.

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Regarding Claim 8, Matsuda et al. teach the device as taught in Claim 7, according to the appropriate paragraph above. Matsuda et al. do not teach a first bonding operation for bonding the first and second element and a second-bonding operation for bonding the first and second conductor pattern, respectively. It is well known in the art to use separate bonding processes for bonding wires, to provide the ability to interchange parts before the final bonding process. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a first and second bonding process in the device of Matsuda et al., to customize the photosensor-amplifier device with specific amplification characteristics during the production process.

10. Claims 11 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda et al. in view of Nishiyama US Patent No. 5,610,395.

Regarding Claims 11 and 14, Matsuda et al. teach the claim limitations of Claim 1, according to the appropriate paragraph above. Matsuda et al. also teach the first and second bonding wire as having substantially identical lengths (see Fig. 3a and 3b) and therefore, a distance between the first electrode and the first input terminal substantially identical to a distance between the second electrode and the second input terminal. Matsuda et al. further teaches the photoelectric conversion circuit as located on a first chip (see Fig. 3a and 3b). Regarding Claim 14, Matsuda et al. teach (see Fig. 3b) a substrate (36) on which the photoelectric conversion circuit and the amplifier circuit are mounted, a first conductor pattern (32a) and a second conductor pattern (32c) formed on the substrate, where the first bonding wire connects the first electrode to the first input terminal (left end of (32a)) by way of the first

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conductor pattern (strip of (32a)) and the second bonding wire connects the second electrode to the second input terminal (right end of (32c)) by way of the second conductor pattern (strip of (32c)). Matsuda et al. do not teach the amplifier circuit on a second chip. Nishiyama teaches (see Fig. 1) a photodetector module with a first chip (2,3) containing a photoelectric conversion circuit and a second chip (4) having an amplifier circuit, wherein the first and second chips are connected by bonding wires (22, 23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a second chip to contain the amplifier circuit as taught by Nashiyama in the device of Matsuda et al., to provide a modular design to enable simple removal and replacement of each chip for upgrade or repair purposes.

Regarding Claim 13, Matsuda et al. teach (see Fig. 4) a photosensor-amplifier device comprising a first chip (see Fig. 3a and 3b) having a photoelectric conversion element (20) that converts an optical signal into an electric signal, a first electrode (30c) on the first chip connected electrically to the photoelectric conversion element, a second electrode (30a) formed on the first chip so as in close proximity to the first electrode, an amplifier circuit (44) (see Col. 6, lines 23-29) for amplifying and outputting a difference between electric signals fed thereto (see Col. 6, lines 23-29), a first input terminal (32c) formed on the amplifier circuit and connected electrically to one input portion of the amplifier circuit, a second input terminal (32a) formed on the amplifier circuit so as to be located in close proximity to the first input terminal and connected electrically to another input portion of the amplifier circuit, a first bonding wire (26c) (see Fig. 3a and 3b) connecting the first electrode to the first input terminal and a second bonding wire (26a) connecting the second electrode to the second input terminal. Matsuda et al. also teach the first chip including a first region (around and below (30c)) formed in a top portion of a

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semiconductor substrate (22) of one conductivity type (n-type) (see Col. 5, lines 9-11) by joining a semiconductor (26) of another conductivity type (p-type) (see Col. 5, lines 11-15), a second region (region of (26) and under (26)), sufficiently smaller than the first region, formed in the top portion of the identical semiconductor substrate by joining the semiconductor (24) of another conductivity type, and an insulating film (28) (see Col. 5, lines 18-21) coating a top surface of the first chip, a photodiode formed by removing a part (28c) of the insulating film that coats the first region and by forming the first electrode so as to be made contact with the first region, a dummy photodiode shielded from light formed by removing a part (28a) of the insulating film that coats the second region and by forming the second electrode in such a way that the second electrode is made contact with the second region through the removed part of the insulating film and that the second electrode (30a) covers all of a top portion (26) of the second region. Nishiyama teaches (see Fig. 1) a photodetector module with a first chip (2,3) containing a photoelectric conversion circuit and a second chip (4) having an amplifier circuit, wherein the first and second chips are connected by bonding wires (22, 23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a second chip to contain the amplifier circuit as taught by Nishiyama in the device of Matsuda et al., to provide a modular design to enable simple removal and replacement of each chip for upgrade or repair purposes.

Regarding Claim 15, Matsuda et al. in view of Nishiyama teach the device as taught in Claim 14, according to the appropriate paragraph above. Matsuda et al. and Nishiyama do not teach a first bonding operation for bonding the first and second element and a second-bonding operation for bonding the first and second conductor pattern, respectively. It is well known in the art to use separate bonding processes for bonding wires, to provide the ability to interchange

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parts before the final bonding process. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a first and second bonding process in the device of Matsuda et al. in view of Nishiyama, to customize the photosensor-amplifier device with specific amplification characteristics during the production process.

11. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda et al. in view of Nishiyama, further in view of Sawada.

Matsuda in view of Nishiyama teach the device as taught in Claim 11, according to the appropriate paragraph above. Matsuda et al. also teach the photoelectric conversion element as a photodiode (see Col. 4, lines 28-33) formed on a semiconductor substrate (22) of one conductivity type (n-type) (see Col. 5, lines 9-11) by joining a semiconductor (24) of another conductivity type (p-type) (see Col. 5, lines 11-15) and coating a top surface with an insulating film (28) (see Col. 5, lines 18-21), the first electrode is formed by removing a part (28a) of the insulating film so that the first electrode is made contact with the semiconductor of another conductivity type and the second electrode is formed on the insulating film. Matsuda et al. and Nishiyama do not teach the second electrode as electrically open. Sawada et al. teach (see Fig. 1) a photosensor-amplifier device comprising a photoelectric conversion element (1,5) and amplifier circuit (600) (see Fig. 3) with a first input terminal (V_{in1}) and a second input terminal (V_{in2}) wherein identical bias voltages (V_{PD}) are applied to the first and second input terminals (see Fig. 1). Applicant defines "electrically open" as "not directly connected to the current signal obtained as a result of photoelectric conversion performed in the photodiode chip" (see Page 8, lines 18-20 of the Applicant's specification)- therefore, Sawada et al. teach (see Fig. 1) the

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second electrode electrically open, as the second electrode is connected to the capacitor and is not associated with the photoelectric conversion performed in the photodiode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an electrically open second electrode as taught by Sawada et al. in the device of Matsuda et al. in view of Nishiyama, to provide a base signal in which to provide cancellation of electromagnetic noise.

Response to Arguments

12. Applicant's arguments with respect to claims 1, 2, 4-9, and 11-15 have been considered but are most in view of the new ground(s) of rejection.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (703)306-3441. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (703)308-4852. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7724 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

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March 13, 2003

DAVID PORTA

SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800